UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,495	04/06/2005	Ramanathan Sethuraman	NL 020975	4791

24737 7590 03/08/2007

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
FONG, VINCENT	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/530,495	SETHURAMAN ET AL.	
	Examiner	Art Unit	
	Vincent Fong	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-17* is/are pending in the application.

4a) Of the above claim(s) *13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04-06-2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 01-04-2007.

Claim 6 has been amended.

Claim 13 has been cancelled.

The 35 USC § 112, second paragraph, rejection of claim 6 has been withdrawn based on the amendment to the claim.

The 35 USC § 112, first paragraph and second paragraph, rejection of claim 13 has been withdrawn based on the cancellation of the claim.

Claims 1-12 and 14-17 are rejected.

Claims 1-12 and 14-17 are pending and have been examined.

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-12 and 14-17 stand rejected for reasons set forth in the previous office action.

2. Claims 1-5, 7 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher et al.(USPN 6026479, hereinafter Fisher) in view of Barry et al.(USPN 6735690, hereinafter Barry).

As per Claim 1, Fisher discloses a data processing apparatus (Abstract Line 1, Column 1 lines 10-13), the apparatus comprising:

An instruction memory address generation circuit for outputting an instruction address, Fisher discloses instruction cache includes address decode to decode instruction

address to select corresponding line from the cache (Column 8 lines 41-65), therefore it is inherent that an instruction memory address generation circuit exists in Fisher's invention for outputting an instruction to the decoder in the cache.

An instruction memory system (Figure 2 Element 120,122, Column 5 lines 25-31, 38-40) arranged to output an instruction word (Column 5 lines 25-31, 38-40) addressed by the instruction address, Fisher discloses using the instruction address bits to perform tag check in the cache to output the correspond line to output (Column 8 lines 60-65).

An instruction unit (Figure 2 Element 150A-D as a whole, Column 2 Line 63-66), arranged to process a plurality of instruction from the instruction word (Column 3 Line 55 – Column 4 Line 5) in parallel (Abstract lines 1-10).

And Fisher discloses a way to control how the instruction execution unit parallelizes processing of the instruction word from the instruction word by supplying the CPU an interrupt(Column 6 lines 38-47).

Fisher does not disclose an detection unit to detect range of instruction address and generate interrupt according to the detected range of instruction address.

However, Barry discloses the above limitations (Column 1 lines 44-45), where "generalized eventpoint mechanism" is the detection unit because it allows the user to define a group of event (includes if an instruction address occurred) to detect and define a group of action (includes generating an interrupt) to take in the event of such detections (Abstract lines 4 to 15). Barry's invention include multiple register to define multiple event(Figure 4 Element 410, Column 8 lines 15-20), also it is possible to

specify a range of instruction address to generate interrupt by using mask register (Column 25 lines 5 –12).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Fisher's inventions to incorporate Barry's inventions so the detection unit disclosed by Barry will detect the range of instruction address and generate interrupt according to switch between high/low ILP mode in Fisher's invention. One of ordinary skill in the art would be motivated to include a detection unit (Barry Column 1 line 44-45) which is providing a common and flexible design for all different type of functions often needed by the processor (Column 2 lines 4-13, 33-41).

As per claim 2, the rejection of claim 1 is incorporated and Fisher further discloses: Instruction memory system (Figure 2 Element 120,122, Column 5 lines 25-31, 38-40) is arranged to adjust a width of the instruction word that determines a number of instruction from the instruction word that is processed in parallel (Column 5 line 62-67 and Column 6 line 55 –63) depends on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose such generating interrupt dependent on detected instruction range.

However, Barry discloses the above limitations. See rejection of Claim 1.

As per claim 3, the rejection of claim 1 is incorporated and Fisher further discloses:

The instruction execution unit (Figure 2 Element 150A-D as a whole, Column 2 Line 63-66) comprises a plurality of functional unit (Figure 2 Element 150A,B,C,D, Column 2 Line 63-66), the instruction execution unit being arranged to select a subset of the functional unit that is available for processing the instructions (Column 7 lines 15 –36) depend on the interrupt received that switch between high/low ILP mode(Column 6 line 38-47). Depending on the ILP mode, some of the execution unit would be dormant and unavailable to execute instructions (Column 7 lines 15 –36).

Fisher does not disclose generating interrupt based on detected range.

However, Barry discloses the above limitations. See rejection of Claim 1.

As per claim 4, the rejection of claim 1 is incorporated and Fisher further discloses:

The instruction execution unit (Figure 2 Element 150A-D as a whole, Column 2 Line 63-66) comprises a plurality of functional unit (Figure 2 Element 150A,B,C,D, Column 2 Line 63-66), the instruction execution unit being arranged to select whether functional units or groups of functional unit from a set of functional unit each receive respective instructions from the instruction word, or receive a shared instruction from the instruction word (Column 5 lines 63-67, Column 6 lines 55-56) depend on the interrupt received that switch between high/low ILP mode(Column 6 line 38-47). In high ILP mode, execution unit 150 A-D will all received instruction from the instruction word, while in low ILP mode, only execution unit 150 D will receive instruction from instruction word (Column 5 lines 63-67, Column 6 lines 55-56).

Fisher does not disclose generating interrupt based on detected range.

However, Barry discloses the above limitations. See rejection of Claim 1.

As per claim 5, the rejection of claim 2 is incorporated and Fisher further discloses: The instruction memory comprises a first memory unit (Figure 2 Element 120) and a second memory unit (Figure 2 Element 122), providing storage with a first (Column 5 lines 26-33) and second (Column 3 lines 2-3) unit of width of addressable memory locations for instruction words of different lengths with addresses in a first and second range respectively (Column 7 Line 15-26), the first and second unit of width being mutually different. In Fisher's invention the first memory unit store multiple execution unit instruction as an instruction word, while the second memory unit store single execution unit instruction as an instruction word therefore they are instruction words of different lengths. Also the compiled code are store into first or second memory unit according to their ILP, therefore it is inherent that the first and second memory unit with address in a first and second range respectively.

As per claim 7, the rejection of claim 5 is incorporated and Fisher further discloses: A memory mapping unit arranged to map the instruction address (Column 7 lines 26-32) onto the first memory unit (Figure 2 Element 120) or the second memory unit (Figure 2 Element 122) dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47). In high (low) ILP mode, the first memory unit (second memory unit) will remain active and memory access will be mapped to the active unit. Fisher does not disclose generating interrupt dependent on detected instruction range.

However, Barry discloses the above limitations. See rejection of Claim 1.

As per claim 15, Barry discloses:

Using an instruction address to fetch an instruction word (Column 8 lines 60-65);

Executing instruction from the fetched instruction word (Column 5 lines 26-36);

Controlling a way in which instruction execution is parallelized dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose an detection unit to range of instruction address and generating interrupt dependent on the detected range of instruction address.

However, Barry discloses the above limitations (Column 1 lines 44-45), where "generalized eventpoint mechanism" is the detection unit because it allows the user to define a group of event (includes if an instruction address occurred) to detect and define a group of action (includes generating an interrupt) to take in the event of such detections (Abstract lines 4 to 15). Barry's invention include multiple register to define multiple event(Figure 4 Element 410, Column 8 lines 15-20), also it is possible to specify a range of instruction address to generate interrupt by using mask register (Column 25 lines 5 –12).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Fisher's inventions to incorporate Barry's inventions so the detection unit disclosed by Barry will detect the range of instruction address and generate interrupt according to switch between high/low ILP mode in Fisher's invention. One of ordinary skill in the art would be

motivated to include a detection unit (Barry Column 1 line 44-45) which is providing a common and flexible design for all different type of functions often needed by the processor (Column 2 lines 4-13, 33-41).

As per claim 16, the rejection of claim 15 is incorporated and Fisher further discloses: Adapting a width of the fetched instruction word (Column 5 line 62-67 and Column 6 line 55 –63) dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose generating interrupt dependent on detected range of instruction address.

However, Barry discloses a detection unit. See rejection of Claim 15.

As per claim 17, the rejection of claim 15 is incorporated and Fisher further discloses: Changing a selection of functional unit of the apparatus that is used to execute the instruction (Column 5 lines 62-67, Column 6 lines 1-25, Column 7 lines 15 –36) dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose generating interrupt dependent on detected range of instruction address.

However, Barry discloses a detection unit. See rejection of Claim 15.

3. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher in view of Barry as applied to claim 5 above, and further in view of Lilja et al. (Exploiting the parallelism available in loops, IEEE Computer, February 1994)(hereinafter Lilja).

As per claim 6, the rejection of claim 5 is incorporated and Fisher further discloses: Longer instruction words (Column 5 lines 26-33) with higher ILP of the program being stored in the first memory unit (Column 7 lines 17-21), shorter instruction words (Column 3 lines 2-3) with lower ILP of the program being stored in the second memory unit (Column 7 lines 22-26), the first unit of width being larger than the second unit of width (Column 5 lines 26-33, Column 3 lines 2-3).

Fisher and Barry do not disclose what type of code would have high/low ILP. However, Lilja discloses that loops comprise larger portion of parallelism (Page 1 lines 15-16).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Fisher's inventions to incorporate Lilja's disclosure. One of ordinary skill in the art would be motivated to exploit loop's parallelism by placing them into the first memory unit due to the abundance of compiling technique to increase the ILP of loop during execution (Page 1 lines 23-26).

As per claim 14, the rejection of claim 1 is incorporated and Fisher further discloses: A method of programming a data processing apparatus, method comprising:

Generating a program of machine instructions for the apparatus (Column 7 lines 15-37);

Identifying high ILP portion of the program (Column 7 lines 15-37);

Loading the program into instruction memory system, so that instructions with high ILP are loaded at memory location with instruction address in a range of address for which the apparatus provides a higher degree of parallelism than another range of addresses(Column 7 lines 15-37).

Fisher and Barry do not disclose what type of code would have high/low ILP.

However, Lilja discloses the above limitations. See rejection of Claim 6.

4. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher in view of Barry as applied to claim 5 above, and further in view of Maiyuran et al. (US PGPub 2002/0129201 A1, hereinafter Maiyuran).

As per claim 8, the rejection of claim 5 is incorporated and Fisher further discloses:

The instruction memory system(Figure 3 Element 120,122) is arranged to power down (Column 7 lines 15-36, Column 8 lines 21-25) the first memory unit(Figure 3 Element 120) dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose that generating interrupt dependent on the detected range of instruction address and powering down unit by disable supply of clock signal to the unit.

However, Barry discloses a "generalized eventpoint mechanism" that is the detection unit because it allows the user to define a group of event (includes if an instruction

address occurred) to detect and define a group of action (includes generating an interrupt) to take in the event of such detections (Abstract lines 4 to 15). Barry's invention include multiple register to define multiple event(Figure 4 Element 410, Column 8 lines 15-20), also it is possible to specify a range of instruction address to generate interrupt by using mask register (Column 25 lines 5 –12).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Fisher's inventions to incorporate Barry's inventions so the detection unit disclose by Barry will detect the range of instruction address and generate interrupt according to switch between high/low ILP mode in Fisher's invention to power down unit dependent on detected range. One of ordinary skill in the art would be motivated to include a detection unit (Barry Column 1 line 44-45) which is providing a common and flexible design for all different type of functions often needed by the processor (Column 2 lines 4-13, 33-41).

Fisher and Barry do not disclose powering down unit by disable supply of clock signal. Further, Maiyuran discloses memory system that power down module depending on the instruction that is processing by the memory system (Abstract lines 2-5). The determination of unit power down depends on the address of the instruction in process (Paragraph 0015). The system power down the module of memory by disable the clock signal to the memory module (Paragraph 0028).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Fisher and Barry's inventions to incorporate Maiyuran's inventions so the system of Fisher and

Barry will power down dormant memory unit by disable the supply of clock signals. One of ordinary skill in the art would be motivated to achieve power saving by powering down unused memory module on a instruction by instruction basis (Paragraph 0013).

As per claim 9, the rejection of claim 5 is incorporated and Fisher further discloses:
The instruction memory system(Figure 3 Element 120,122) is arrange to power down (Column 7 lines 15-36, 62-67, Column 8 lines 1-7, 21-25) all memory unit but the memory with the requested instruction dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).
Fisher does not disclose that generating interrupt dependent on the detected range of instruction address and powering down unit by disable supply of clock signal to the unit.
However, Barry discloses a detection unit (Column 1 lines 44-45). See rejection of Claim 8.
Fisher and Barry do not disclose that powering down unit by disable supply of clock signal.
Further, Maiyuran discloses the above limitations. See rejection of Claim 8.

5. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher in view of Barry as applied to claim 2 above, and further in view of Sanches et al. (US PG Pub 2002/0116596 A1, hereinafter Sanches).
As per claim 10, the rejection of claim 2 is incorporated and Fisher further discloses:

Instruction memory system (Figure 2 Element 120,122, Column 5 lines 25-31, 38-40) comprises a plurality of memory units, each arranged to be responsive (Column 7 lines 15-36, 62-67, Column 8 lines 1-7, 21-25) dependent on the interrupt that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose generating interrupt dependent to instruction address range and it doesn't arrange the system instruction word as a combination from memory units. However, Barry discloses a "generalized eventpoint mechanism" that is the detection unit because it allows the user to define a group of event (includes if an instruction address occurred) to detect and define a group of action (includes generating an interrupt) to take in the event of such detections (Abstract lines 4 to 15). Barry's invention include multiple register to define multiple event(Figure 4 Element 410, Column 8 lines 15-20), also it is possible to specify a range of instruction address to generate interrupt by using mask register (Column 25 lines 5 –12).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Fisher's inventions to incorporate Barry's inventions so the dectection unit disclose by Barry will detect the range of instruction address and generate interrupt according to switch between high/low ILP mode in Fisher's invention. One of ordinary skill in the art would be motivated to include a detection unit (Barry Column 1 line 44-45) which is providing a common and flexible design for all different type of functions often needed by the processor (Column 2 lines 4-13, 33-41).

Fisher and Barry do not disclose arrangement of the system instruction word as a combination from memory units.

Further, Sanches discloses a instruction memory system that comprises a plurality of memory units each responsive to some instruction address (Abstract lines 3-6). The instruction allow overlap of address range (Paragraph 0042, Table 2), all memory unit can response to the same memory address (overlap) while contain only part of the data for the address. The system is arranged to supply instruction word as a combination of instructions from those memory units (Abstract lines 8-13Paragraph 0028, 00042).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Fisher and Barry's inventions to incorporate Sanches's inventions. One of ordinary skill in the art would be motivated to save memory space by excluding NOP from the code (Paragraph 0015).

As per claim 12, the rejection of claim 10 is incorporated and Fisher further discloses:

The instruction execution unit (Figure 2 Element 150A-D as a whole, Column 2 Line 63-66) comprises groups of one or more functional unit (Figure 2 Element 150A,B,C,D, Column 2 Line 63-66), each group being coupled to a respective predetermined one of the memory unit(Column 5 lines 26-53, Column 7 lines 14-36), for receiving instructions from the instruction words depend on the interrupt received that switch between high/low ILP mode(Column 6 line 38-47).

Fisher does not disclose generating interrupt based on detected range.

However, Barry discloses a detection unit. See rejection of Claim 10.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher in view of Barry in further view of Sanches as applied to claim 10 above, and further in view of Maiyuran.

As per claim 11, the rejection of claim 10 is incorporated and Fisher further discloses:

The instruction memory system (Figure 3 Element 120,122) is arrange to power down (Column 7 lines 15-36, 62-67, Column 8 lines 1-7, 21-25) at least one memory unit when instruction address does not fall on that memory dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose that generating interrupt dependent on the detected range of instruction address and powering down unit by disable supply of clock signal to the unit.

Barry discloses a detection unit. See rejection of Claim 8.

Fisher and Barry do not disclose that powering down unit by disable supply of clock signal.

Further, Maiyuran discloses the above limitations. See rejection of Claim 8.

Response to Arguments

7. Applicant's arguments filed 01-04-2007 have been fully considered but they are not persuasive. In remarks, the applicant argues in substance:

(1) The '690 patent (Barry et al. USPN 6735690) does not describe detecting a range of an instruction address and controlling the way execution units parallelize processing of an instruction based on an address range of the instruction.

Response

(1) Examiner believes that the '690 patent does in fact teach," detecting a range of an instruction address".

The '690 patent teaches that using single address and masking in the address comparasion, it support multiple address matching. It can be use to trapping when access to specified regions of memory (range of instruction address). (Column 25 lines 5-12). In addition 690' teaches multiple definable address register (Figure 4 element 410) for address detecting, thus detecting a range of instruction address is possible wit the use of multiple instruction data point (column 8 lines 15-20).

Examiner believes that the 690' patent teach, "generation of interrupt based on an address range of the instruction."

479' patent (Fisher et al. USPN 6026479) teaches controlling the way execution units (element 154 A-D figure 2) parallelize processing; switching between high and low ILP mode, an instruction based on interrupts (Column 6 lines 38-47), it does not teach the generation of interrupts are based on the range of the instruction. However 690' patent teaches the generation of interrupt based on an address range of the instruction; define processor event in the register (Figure 4 element 410) to check if an instruction address occur (abstract) and to generate a processor action to cause generation of interrupt (abstract), also multiple processor event could be defined in the multiple

register provided (figure 4 element 410, column 8 lines 15-20) and (detecting a range of instruction address; multiple addressing matching, is enable by the use of address masking (column 25 lines 5-12). It is the obvious combination of the two patents that teaches "controlling the way execution units parallelize processing of an instruction based on an address range of the instruction".

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Fong whose telephone number is 571-270-1409. The examiner can normally be reached on 7:00-3:30 Mon - Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Fong VF
February 28 2007

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100